Claims 13, 15, 22, 24 and 31 have been amended to correct typographical errors in the terms "M" or "N."

Claims 11, 32, 33 and 35 are rejected under 35 U.S.C. §112 as being indefinite in the use of the phrase "a portion" of a signal and in the recitation of "the next data message" in claim 35. Claims 11 and 32 have been amended to change "a portion" to --data bits-- or --bits-- and, in claim 35, "the next data message" has been changed to --a next data message--. It is submitted that, as amended, each of the claims is now clear and definite.

Claims 1-36 are rejected, either under 35 U.S.C. §102 as being anticipated by patent no. 5,333,114 to Warrior et al., or under 35 U.S.C. §103 as being unpatentable over Warrior et al. in view of patent no. 6,117,010 to Canterbury et al. Warrior et al. discloses a control system for a petrochemical tank farm, while Canterbury et al. is cited for a teaching of a gaming device which includes optical LED devices and switch devices. The rejections are respectfully traversed.

Each of the independent claims 1, 13, 24 and 31, recites "a gaming system" or a method for individually accessing a plurality of devices "in a gaming system". Warrior et al. does not disclose or suggest a gaming system and, therefore, for this reason alone, cannot anticipate any of applicant's claims.

More importantly, each of the independent claims recites "a host controller" and "a plurality of local controllers," or plural nodes each including a local controller, the controllers being interconnected serially or in a string "with the data out terminal of the host controller being connected to the data in terminal of a first local controller [or node] and the data in terminal of each of the other local controllers [or nodes] being connected to the data out terminal of the preceding local controller [or node]", wherein each of the local controllers or nodes is connected

to plural devices to be controlled. No such arrangement is disclosed or suggested by the cited art.

The examiner contends that Warrior et al. discloses a plurality of local controllers (supervisory master units 10) "being interconnected in a string" using the specific interconnection recited in the claims. No such arrangement is disclosed or suggested by Warrior et al. While Warrior et al. does suggest plural supervisory master units 10 (column 3, lines 21-23), there is no suggestion whatsoever that they be connected in a string. Rather, Warrior et al. clearly suggests that they would be connected in parallel to the master controller 6, suggesting that each would require its own cable running to the control room 36 (see column 3, lines 29-30).

Furthermore, there is no suggestion at all in Warrior et al. that any of its supervisory master units 10 has "a data in terminal", a "data out terminal", a "power line" and a "common line" as required by claim 1.

Furthermore, each of claims 13, 24 and 31 requires that the string of nodes or local controllers cooperate to provide a "(MxN)-bit shift register." No such arrangement is disclosed or suggested by Warrior et al., nor does the examiner contend otherwise.

None of the foregoing features is supplied by Canterbury et al.

For all of these reasons, it is submitted that, as amended, each of the remaining claims 1-36 is now in condition for allowance and the allowance thereof is respectfully asked.

Respectfully submitted,

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By J. Jerry Steinman

Version of Abstract to Show Changes Made

A system controls access to [a plurality of] plural devices with only four lines by grouping the devices in nodes, [wherein] each node [includes a local control circuit and] including a predetermined number of the devices, [with each] and a local control circuit defining a shift register[, the] with positions [of which are] respectively connected to the devices. The nodes are connected in series with a host controller, [so that the shift registers of the several nodes cooperate] to form a system shift register. The nodes are serially addressed by a serial data message from a DATA OUT line of the host controller, which message includes MxN data bits followed by strobe indicator, where N is the number of nodes and M is the number of devices at each node. All controllers are connected to a V+ line and a COMMON line and a RETURN line. The system register forms a fourth line, with one end [of which is] connected to the host controller DATA OUT terminal and the other end [of which may be connected] connectable to the RETURN line.

Version of Claims Marked to Show Changes Made

11. (Amended) The gaming system of claim 8, wherein the devices include switches and LEDs, the output signal including [a portion] data bits for causing the local controllers to record the states of the switches and [a portion] data bits for causing the local controllers to control the states of the LEDs.

13. (Amended) A gaming system comprising:

a plurality of devices to be individually accessed, arranged in a string of [M] N nodes, with each node including up to [N] M of the devices, wherein M and N are whole numbers greater than one;

a host controller having a data out terminal;

a plurality of local controllers respectively associated with the nodes,

each local controller having a data in terminal and a data out terminal and including a [N-bit] M-bit shift register with the register positions respectively connected to device output terminals to which the devices of the associated node may respectively be connected;

the data out terminal of the host controller being connected to the data in terminal of a first node and the data in terminal of each of the other nodes being connected to the data out terminal of the preceding node in the string so that the string of nodes provides a (MxN)-bit shift register;

the host controller producing at its data out terminal an output signal comprising a serial digital data stream including MxN bits followed by a strobe indicator so that the MxN bits are sequentially loaded into and fill the (MxN)-bit register;

each local controller being responsive to the strobe indicator for utilizing the contents of its [N-bit] M-bit register for accessing the associated devices.

15. (Amended) The gaming system of claim 14, wherein [N] M is 4.

21. (Amended) The gaming system of claim 13, wherein the output signal is comprised of bytes each having [a length of $(N)2^x$ bits] at least one M-bit segment.

22. (Amended) The gaming system of claim 21, wherein consecutive [N-bit] M-bit segments of a byte respectively address consecutive nodes.

24. (Amended) A gaming system comprising:

a plurality of devices to be individually accessed including one or more first devices to be sensed and one or more second devices to be controlled, the devices being arranged in a string of [M] N nodes with each node including up to [N] M of the devices, wherein M and N are whole numbers greater than one;

a host controller having a data out terminal and a data in terminal;

a plurality of local controllers respectively associated with the nodes,

each local controller having a data in terminal and a data out terminal and including a [N-bit] M-bit shift register with the register positions respectively connected to device output terminals to which the devices of the associated node may respectively be connected;

the data out terminal of the host controller being connected to the data in terminal of a first node and the data in terminal of each of the other nodes being connected to the data out terminal of the preceding node in the string so that the string of nodes provides a (MxN)-bit shift register, and the data out terminal of a last node being connected to the data in terminal of the host controller;

the host controller producing at its data out terminal an output signal comprising a serial digital data stream including MxN bits followed by a strobe indicator so that the MxN bits are sequentially loaded into and fill the (MxN)-bit register,

each local controller being responsive to the strobe indicator for: (a) for each of its register positions connected to a first device, loading into that register position a bit indicative of the current state of the first device; and (b) for each of its register positions connected to a second device, latching the contents of that position to its associated device output terminal for controlling the associated second device.

31. (Amended) A method for individually accessing each of a plurality of devices in a gaming system comprising:

grouping the devices into [M] N nodes, with each node including a local controller and up to [N] M devices connected to the local controller, wherein M and N are whole numbers greater than one,

connecting the local controllers in series with one another and with a data out terminal of a host controller so that the local controllers cooperate to define an (MxN)-bit shift register,

providing a power line connected to all of the controllers and a common line connected to all of the controllers, and

transmitting from the host controller data out terminal to all of the local controllers a serial digital data message including MxN bits respectively corresponding to the devices for individually controlling the devices.

32. (Amended) The method of claim 31, wherein the data message terminates with a strobe indicator which causes each local controller to access the devices connected thereto in accordance with [a portion] bits of the data message corresponding to that local controller.

35. (Amended) The method of claim 34, wherein each digital data message terminates with a strobe indicator, and each local controller responds to the strobe indicator for storing, for each at least one device connected thereto, a data bit corresponding to the current

state of the at least one device, the stored bits being shifted from the register in response to [the] a next data message from the host controller.